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FEL

TNO Physics and Electronics Laboratory

P.O. Box 9
2509 JG
Oude Waal
The Hague, The Netherlands

Fax +31 70 328 09 61
Phone +31 70 326 42 21

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A Real-time Synthetic Aperture Radar Processor: Introduction and Project Description

author(s):

L.H.J. Bierens

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institute : TNO Physics and Electronics Laboratory

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Research supervised by : H.R. van Es
Research carried out by : L.H.J. Bierens

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ABSTRACT (Unclassified)

This report presents a project description for the design and realization of a real-time synthetic aperture radar (SAR) processor. The principles of SAR processing and the state of the art are described. Conventional SAR processing techniques depend largely on FFT transformation techniques and devices. These offer limited possibilities to increase speed and performance of a SAR processor. Therefore the design of new algorithms rather than architectures for existing algorithms is suggested. After that new architectures will be designed dedicated to the new algorithms. By exploring parallel structures of the algorithms and by using VLSI array processing, speed and performance can be increased significantly. The intention is that the project will lead to a PhD graduation.

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SAMENVATTING (Ongerubriceerd)

Dit rapport bevat een project beschrijving voor het ontwerpen en realiseren van een real-time synthetic aperture radar (SAR) processor. De principes van SAR processing en de huidige stand van zaken worden beschreven. Conventionele SAR processing technieken zijn grotendeels gebaseerd op FFT- transformatietechnieken en -devices. Deze bieden beperkte mogelijkheden om snelheid en performance van een SAR processor te verbeteren. Gesuggereerd wordt om in de eerste plaats nieuwe algoritmen te ontwerpen in plaats van architecturen voor bestaande algoritmen. Pas in de tweede plaats zullen nieuwe architecturen worden ontworpen toegespitst op de nieuwe algorithmen. Door gebruik te maken van parallelle structuren van algoritmen en van VLSI array processing, kunnen naar verwachting snelheid en performance aanzienlijk verbeterd worden. Het ligt in de bedoeling dat het onderzoek zal leiden tot een promotie.

LIST OF SYMBOLS

c:	speed of light (meters/second)
D:	physical aperture length (meters)
h:	height of the aircraft (meters)
L:	synthetic aperture length (meters)
M:	number of samples of a compressed pulse
N:	number of succesive pulses that forms a synsthetic aperture
R:	distance between antenna at t_n and point target at $(x_0, y_0, 0)$ (meters)
R':	distance between antenna at t_n and point target at $(x, y, 0)$, with $(x, y, 0)$ nearby $(x_0, y_0, 0)$
R_0:	distance between antenna at t_0 and point target at $(x_0, y_0, 0)$ (meters)
t:	time (seconds)
T:	interpulse time (seconds)
v:	velocity of the aircraft (meters/second)
Δv:	along track velocity error (meters/second)
v_r:	across track velocity error (meters/second)
$\mathbf{v}_n$:	vector containing samples of the echo of the n^{th} pulse after pulse compresion
x_n:	x-coordinate antenna position at t_n (meters)
α:	chirprate (radians/second)
β:	physical beamwidth (radians)
β_{synth}:	synthetic beamwidth (radians)
δ_a:	azimuth resolution (meters)
δ_r:	range resolution (meters)
λ:	wavelength of carrierwave (meters)
τ:	pulse width (seconds)
τ_c:	pulse width compressed pulse (seconds)
ω_c:	angular frequency carrier wave (radians/second)

1 INTRODUCTION

1.1 VLSI array processing for SAR

Present-day applications of digital signal processing increasingly demand high speed and performance processing systems. To satisfy these demands two points of view can be distinguished. The first one is to ensure that a processing system keeps up with the demands, irrespective of the type of application. The second one is to decrease the complexity of the digital signal processing algorithms, irrespective of the type of processing system that is used. It is obvious that neither one nor the other will give an optimal performance on its own. However, a combination of both will probably do.

A useful approach in the design of digital signal processing systems for a dedicated application is to start with an expedient analysis of the application fields. Hereby one has to have already in mind some alternative processor types for this particular application. Examples are: array processors, general purpose digital signal processors and application specific processors. The question whether the system should be software or hardware oriented must be answered. I.e. the boundaries of the application field as a whole have to be defined. Then an algorithm is designed, which is optimized for this application and its field. The next step is the design of an architecture which is optimized for the algorithm within the boundaries of the application field. Then the sytem is implemented, i.e. the architecture is mapped on some hard- or software components.

An application digital signal processing is synthetic aperture radar (SAR) processing. A SAR is an imaging radar on a moving platform, in general an aircraft or satellite. SAR processing is based on synthetic generating of an effective long antenna by signal processing rather than using a long physical antenna. The amount of SAR data which has to be processed to generate an image is so high that high speed, high performance and low cost processing is hardly possible. Due to the progress in (VLSI) digital signal processing techniques, real-time high performance and low cost SAR processing systems come within reach. Because of this reason the Physics and Electronics Laboratory, as a leading institute on radar technology, decided to design a real-time on-board aircraft SAR processor.

Within the application field (SAR processing) two mayor requirements can be distinguished directly. The processor must be real-time and it must be an on-board system. The first requirement demands high processing speed and the second one demands restrictions on the size of the processor and its power consumption. A VLSI type array processor is, probably, the best implementation to meet these requirements. The quality of the image must be at least such that the flight can be judged as successful or not. VLSI array processor design for real-time SAR processing is a relatively new subject. Therefore the first step of the design trajectory is the design of algorithms (as stated above). VLSI array processing requires algorithms that have low computational complexity and a high degree of parallelism. The second step is to map the resulting algorithms onto architectures. Requirements for the architecture are a high degree of regularity and parallelism.

1.2 SAR processing for VLSI array processors

Traditionally SAR processing algorithms can be divided in two mayor parts: range compression and azimuth compression. Range compression is a signal processing approach that increases the resolution in range direction (across the movement trajectory). The resolution in range depends mainly on the pulse width. An ideal pulse would be a narrow pulse with high peak power, such that a good signal-to-noise (S/N) ratio is achieved. In practice such a system is not feasible. An alternative is to transmit a relatively long pulse with low peak power, but with high average power. After receiving the echo it is compressed to a narrow pulse with high peak power. Azimuth compression is a signal processing approach to increase the resolution in azimuth direction (along the movement trajectory). A single pulse radar would have a resolution in azimuth that depends on the beamwidth and the distance between antenna and ground. By processing successive echoes the azimuth resolution is increased significantly, and becomes also independent of the distance between antenna and ground. Range and azimuth processing are mathematically equivalent techniques.

Besides range and azimuth compression also phase error compensation is of great importance in SAR processing. Phase errors are caused by, for example, uncontrolled motions of the moving platform, atmospherical losses, etc.. These effects cause, among others,

blurring and defocussing of the image, which will result in a lower resolution. Phase errors can be estimated and compensated by several image processing and signal processing techniques. In general this will be done after range and azimuth compression. In this report a few examples will be given, but details and a broad outline of possible techniques can be found in the references.

Traditional algorithms for range and azimuth compression and phase error compensation have high complexity and use large storage facilities. This implies much processing time, large processing and storage equipment and much overhead for memory management, processing control, etc.. Untill now SAR processing is performed off-line and off-board, and the main requirement is to achieve high resolution. Therefore little effort is given to increase the performance, for example by designing new algorithms. An exception is made for phase error estimation and compensation algorithms, but the reason for this is not a desired increase of perormance but an increase of resolution.

As stated before real-time high performance SAR processing comes within reach because of the progress in VLSI array processing techniques. Due to the high complexity, traditional SAR processing algorithms, and thus architectures, are not suitable for implementation on VLSI array processors. Hence new algorithms and architectures dedicated to VLSI array processing must be designed, as an alternative for traditional algorithms for range and azimuth compression and phase error compensation.

1.3 Outline

This report describes the design project of a real-time on-board SAR processor. New algorithms and architectures will be designed to perform SAR processing. These algorithms and architectures must be dedicated to VLSI array processing systems. The intended result of the project will be the definition, design and realization of a real-time on-board SAR processor. The necessary research for this project will be carried out in cooperation with the Delft University of Technology, faculty of Electrical Engineering, section Network Theory. It is the intention that this research will also lead to a PhD graduation.

The organization of this report is as follows. Chapter 2 gives the background theory of SAR processing. The conventional approach of SAR processing is shortly outlined, and a discussion of the state of the art is given. A short introduction of the Physics and Electronics Laboratory and the position of this project in it is given. Chapter 3 defines the project. Objectives, intended results and the requirements are outlined and the sub-projects are defined. The project stages and its activities are defined and described in chapter 4. Chapter 5 gives the time planning, information flows and organization and defines quality norms. Finally, chapter 6 describes the planning and activities for the research, which has to lead to a PhD graduation.

2 BACKGROUND

2.1 Synthetic aperture radar theory

Synthetic aperture radar. A synthetic aperture radar (SAR) is a side-looking imaging radar on a moving platform [1, 15, 18, 20, 26, 29]. Usually the platform is a satellite (spaceborne SAR) or aircraft (airborne SAR). SAR is based on synthetic generating of an effective long antenna by signal processing rather than using a long physical antenna. The actual physical antenna length is in most cases relatively small. With the synthetic antenna a narrow beam in azimuth can be achieved, and thus a higher resolution, relative to the actual physical antenna. Let the physical antenna length be D and the wavelength of the transmitted signal λ than the physical half-power beamwidth in radians is given by:

$$\beta = \frac{\lambda}{D} \tag{2.1}$$

If L is the length of the synthetic array, with $L \gg D$, then the beam-width of the synthetic antenna is given by [15, 26, 29]

$$\beta_{synt} = \frac{\lambda}{2L} \tag{2.2}$$

Let the distance between the antenna and a point on the ground be R. Then the maximum synthetic aperture length is limited by the length of the illumination pattern of the physical beam on the ground [15, 26]

$$L \leq \frac{R\lambda}{D} \tag{2.3}$$

This gives for the maximum resolution in azimuth (parallel to the flight trajectory), δ_a, the expression

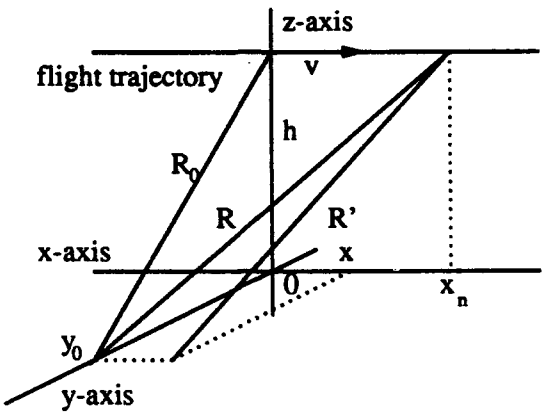

Figure 2.1: Geometry of the SAR system.

$$\delta_a = \beta_{synt} R = \frac{D}{2} \tag{2.4}$$

while for the real aperture the maximum resolution would be $\beta R = \lambda R/D$. For example in airborne systems, with (in meters) R of order 10^3, D of order 10^{-1} and λ of order 10^{-2}, we have a maximal azimuth resolution of order 10^2 for a real aperture and a resolution of order 10^{-1} for a synthetic aperture. It should also be noticed that the resolution of a synthetic aperture is independent of R and λ. In the rest of the document it will be assumed that, if not stated otherwise, a SAR system is airborne.

Let the transmitted signal be a sequence of pulses. Let $p(t)$ be a single pulse, defined in the interval $(-\tau/2, \tau/2)$ and zero otherwise, with τ the pulse width. Assume that at $t = t_n$, $n = \cdots, -1, 0, 1, \cdots$, a single pulse is transmitted. Let the interpulse time T be relatively large: $T \gg \tau$, and let the carrier frequency be ω_c then the transmitted signal is given as

$$s(t) = \sum_n e^{j\omega_c t} p(t - t_n) \tag{2.5}$$

The geometry of the SAR system is shown in figure 2.1. Let a single unit point scatterer have coordinates $(x_0, y_0, 0)$, and let the height of the flight trajectory be h. Let the dis-

tance between the antenna at $t = t_n$ and the point scatterer be defined as R and define $R_0 = \sqrt{y_0^2 + h^2}$. Notice that R depends on t_n. Furthermore the x-coordinates of the successive positions of the aircraft at $t = t_n$ are defined as $x = x_n$. Assume that $x_0 = 0$ and let v be the velocity of the aircraft, then $x_n = nvT$. Let c be the speed of light then the echo signal of $s(t)$ can be described as

$$s(t - \frac{2R}{c}) = \sum_n e^{j\omega_c(t-\frac{2R}{c})} p(t - t_n - \frac{2R}{c}) \tag{2.6}$$

where $2R/c$ is the round trip time delay of the reflected pulse. Usually the term $e^{j\omega_c t}$ is omitted, since it contains no information of the scatterer. Hence

$$s(t - \frac{2R}{c}) = \sum_n e^{-j\omega_c \frac{2R}{c}} p(t - t_n - \frac{2R}{c}) \tag{2.7}$$

Pulse compression. Pulse compression is a technique to increase the resolution in range (parallel to the y-axis). The resolution in range is determined by the pulse width of the transmitted pulse. The resolution in range without pulse compression is given as $c\tau/2$ [15]. This means that high resolution in range requires a very narrow pulse. At the other hand high pulse power is required to achieve a good S/N ratio. An ideal pulse form would be an approximation of a Dirac pulse. Due to the physical constraints of the transmitter this is not feasible. A solution to this problem is to transmit a linear frequency modulated pulse, a so-called "chirp", defined as

$$p(t) = e^{j\alpha t^2} \tag{2.8}$$

where α is the chirprate. Figure 2.2a shows a chirp. A sequence of relative long pulses is transmitted. After receiving the echo it is subjected to a matched filter. The matched filter compresses the received pulses to very narrow pulses with the same power as the original echo pulse. Let $s_c(t)$ be the echo signal, subjected to the matched filter, then

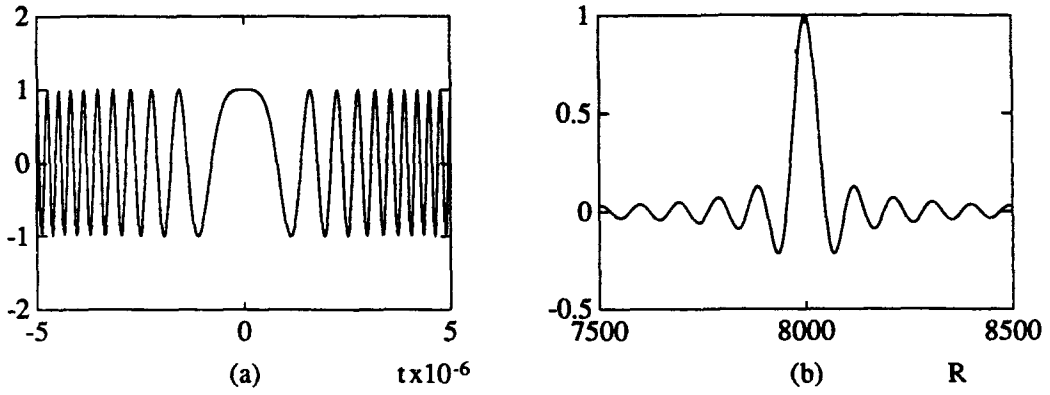

Figure 2.2: (a) Chirp and (b) compressed pulse.

$$
\begin{aligned}
s_c(t) &= \frac{1}{\tau}\int s(t-\frac{2R}{c})s^*(t-\frac{2R'}{c})\mathrm{d}t \\
&= \sum_n e^{-j\omega_c\frac{2(R-R')}{c}}\frac{1}{\tau}\int_{-\tau/2}^{\tau/2} e^{j\alpha(t-t_n-\frac{2R}{c})^2}e^{-j\alpha(t-t_n-\frac{2R'}{c})^2}\mathrm{d}t \qquad (2.9)
\end{aligned}
$$

where * means the conjugate and R' is the distance between the antenna and a point $(x, y, 0)$ nearby $(0, y_0, 0)$, see figure 2.1. Expanding the integral in 2.9 gives

$$
\begin{aligned}
\frac{1}{\tau}\int_{-\tau/2}^{\tau/2} e^{j\alpha(t-t_n-\frac{2R}{c})^2}e^{-j\alpha(t-t_n-\frac{2R'}{c})^2}\mathrm{d}t &\approx e^{j\alpha\frac{4}{c^2}(R^2-R'^2)}\frac{1}{\tau}\int_{-\tau/2}^{\tau/2} e^{-j\alpha\frac{4}{c}t(R-R')}\mathrm{d}t \\
&= e^{j\alpha\frac{4}{c^2}(R^2-R'^2)}\mathrm{sinc}(\alpha\tau\frac{4}{c}(R-R')) \qquad (2.10)
\end{aligned}
$$

The last expression is a compressed pulse with the same pulse power as before the filtering, but with much higher S/N ratio and much smaller pulse width, see figure 2.2b. Then 2.9 becomes[1]

[1] In this expression it is assumed that over the complete aperture the phase change of 2.10 is small according to the phase change $\omega_c\frac{2(R-R')}{c}$, which is only true for short aperture lengths. In real SAR systems however this may cause a phase error (range migration), but in this system the error is assumed neglectable.

$$s_c(t) = e^{j\alpha\frac{4}{c^2}(R^2-R'^2)}\mathrm{sinc}(\alpha\tau\frac{4}{c}(R-R'))\sum_n e^{-j\omega_c\frac{2(R-R')}{c}} \tag{2.11}$$

The pulse width of the compressed pulse τ_c is given by $\tau_c = 2.8/\alpha\tau$ [26]. The range resolution δ_r is then given by

$$\delta_r = \frac{c\tau_c}{2} = \frac{1.4c}{\alpha\tau} \tag{2.12}$$

Azimuth compression. Azimuth compression is the signal processing technique that obtains a high resolution in azimuth from a sequence of echo pulses. From figure 2.1, R' and R are approximated as

$$R' = \sqrt{R_0^2 + (x-x_n)^2} \approx R_0 + \frac{(x-x_n)^2}{2R_0} \tag{2.13}$$

$$R = \sqrt{R_0^2 + x_n^2} \approx R_0 + \frac{x_n^2}{2R_0} \tag{2.14}$$

These approximations are valid if $R \gg x - x_n$ and $R' \gg x_n$, which is true in most cases. Let the synthetic aperture length be L then the number of pulses transmitted during the building of the aperture is given as $N+1 = L/vT$. Then expanding the summation in 2.11 becomes

$$\begin{aligned}\sum_n e^{-j\omega_c\frac{2(R-R')}{c}} &= \sum_{n=-N/2}^{N/2} e^{-j\omega_c\frac{2}{c}\frac{((x-x_n)^2-x_n^2)}{2R_0}} \\ &= e^{-j\omega_c\frac{2}{c}\frac{x^2}{2R_0}} \sum_{n=-N/2}^{N/2} e^{j\omega_c\frac{2}{c}\frac{nvT}{R_0}} \\ &= e^{-j\frac{4\pi}{\lambda}\frac{x^2}{2R_0}} \frac{\sin((N+1)\frac{4\pi}{\lambda}\frac{vT}{2R_0})}{\sin(\frac{4\pi}{\lambda}\frac{vT}{2R_0})}\end{aligned} \tag{2.15}$$

where $x_n = nvT$ and $2\omega_c/c = 4\pi/\lambda$ are used. Figure 2.3a shows the magnitude term of 2.15 as function of x. The azimuth resolution is derived from the half-power bandwidth of 2.15 [26]

$$\delta_a = \frac{1.4\lambda R_0}{\pi L} \tag{2.16}$$

The maximum resolution is obtained by substitution the maximum aperture length $L = R_0\lambda/D$ which gives $\delta_a \approx D/2$. Notice that this value was expected from 2.4. The echo signal after pulse and azimuth compression is thus

$$s_c(t) = \epsilon^{j\alpha\frac{4}{c^2}(R^2-R'^2)} e^{-j\frac{4\pi}{\lambda}\frac{x^2}{2R_0}} \frac{\sin((N+1)\frac{4\pi}{\lambda}\frac{xvT}{2R_0})}{\sin(\frac{4\pi}{\lambda}\frac{xvT}{2R_0})} \mathrm{sinc}(\alpha\tau\frac{4}{c}(R-R')) \tag{2.17}$$

Figure 2.3b shows the magnitude term of the complete filtered echo signal 2.17 as function of x and R'.

Phase errors. In the previous it was assumed that the flight trajectory was a straight line, that the velocity was constant, that no atmospherical losses did occur, etc.. In practical systems this will not be the case, moreover, it results in phase errors in the echo signal. These errors cause unwanted effects on the image, like defocussing. In [18] phase errors are subdivided in two groups: predictable and unpredictable phase errors.

Examples of predictable phase errors are: errors caused by geocoding and range migration. Geocoding is the mapping the SAR coordinate system (the (r, x) coordinate system) onto an image coordinate system (usually the (x, y) coordinate system). An example of the error that can occur is the following. Let R be the distance between the antenna and a target on the ground with coordinates (x, y). Let a nearby target with coordinates $(x, y + \Delta y)$ have distance $R + \delta_r$. The image plane is the (x, y) plane, thus Δy is the actual resolution. Figure 2.4a shows that Δy depends on the angle θ_y, while δ_r is independent of θ_y. This dependency results in a predictable phase error. More examples of errors caused by geocoding can be found in [18]. Range migration is caused by a pulse compression assumption. The distances between successive antenna positions during the

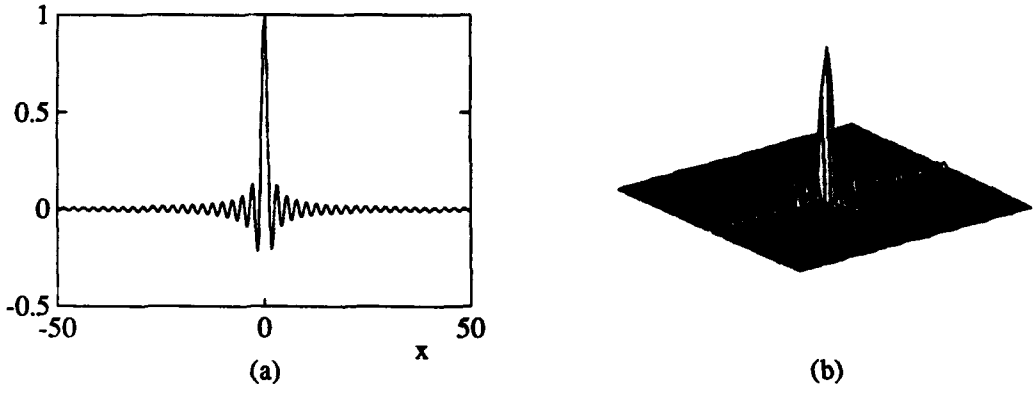

Figure 2.3: (a) Azimuth compression and (b) complete echo signal.

aperture building and a single point target are assumed constant. This is illustrated in figure 2.4b. These distances differs maximally $\sqrt{(\frac{1}{2}L)^2 + R^2} - R$. For long aperture lengths range migration causes relevant phase errors. Since it is completely predictable however, it will be neglected in this section.

Unpredictable phase errors are caused by: unknown ground height variation, atmospheric propagation fluctuations and unknown flight trajectory. From these three the last one causes the most important (unwanted) phase error. An error in the flight trajectory will hardly affect the phase during the round-trip time of a single echo pulse. It will only affect the phase during several pulses. Figure 2.5 shows that the displacement in the flight trajectory can be expressed in range difference as

$$R - R_0 \approx y(t) + \frac{x(t)^2}{2R_0} \tag{2.18}$$

Then the phase shift can be written as

$$\varphi(t) = \frac{4\pi}{\lambda}(y(t) + \frac{x(t)^2}{2R_0}) \tag{2.19}$$

If the displacements are expanded about $t = 0$ then

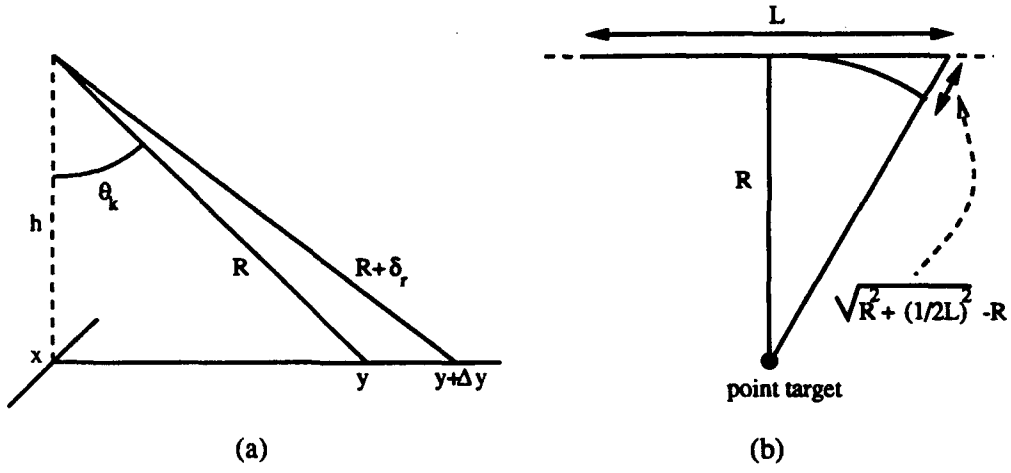

Figure 2.4: (a) Geocoding phase error and (b) range migration.

$$x(t) = (v + \Delta v)t + \frac{1}{2}t^2\frac{\mathrm{d}}{\mathrm{d}t}v + \frac{1}{6}t^3\frac{\mathrm{d}^2}{\mathrm{d}t^2}v + \cdots \tag{2.20}$$

$$y(t) = v_r t + \frac{1}{2}t^2\frac{\mathrm{d}}{\mathrm{d}t}v_r + \frac{1}{6}t^3\frac{\mathrm{d}^2}{\mathrm{d}t^2}v_r + \cdots \tag{2.21}$$

where Δv, $\frac{\mathrm{d}}{\mathrm{d}t}v$, $\frac{\mathrm{d}^2}{\mathrm{d}t^2}v, \cdots$ are along-track velocity errors and v_r, $\frac{\mathrm{d}}{\mathrm{d}t}v_r$, $\frac{\mathrm{d}^2}{\mathrm{d}t^2}v_r$, $\cdots$ are across-track velocity errors. Hence, with the assumption that the terms of fourth-order are neglectable, the phase shift becomes

$$\varphi(t) = \frac{4\pi}{\lambda}\frac{v^2t^2}{2R_0} + \varphi_e(t) \tag{2.22}$$

where

$$\varphi_e(t) = \frac{4\pi}{\lambda}(2\Delta v t^2 + t^3\frac{\mathrm{d}}{\mathrm{d}t}v) + \frac{4\pi}{\lambda}(v_r t + \frac{1}{2}t^2\frac{\mathrm{d}}{\mathrm{d}t}v_r + \frac{1}{6}t^3\frac{\mathrm{d}^2}{\mathrm{d}t^2}v_r) \tag{2.23}$$

Notice that if Δv, $\dot{v}$, v_r, $\frac{\mathrm{d}}{\mathrm{d}t}v_r$, $\frac{\mathrm{d}^2}{\mathrm{d}t^2}v_r = 0$ then $\varphi_e(t) = 0$ and $\varphi(t)$ equals $\frac{4\pi}{\lambda}(R - R')$ in equation 2.9, if R and R' are approximated by 2.13 and 2.14 and $x_n = 0$ and $x = vt$.

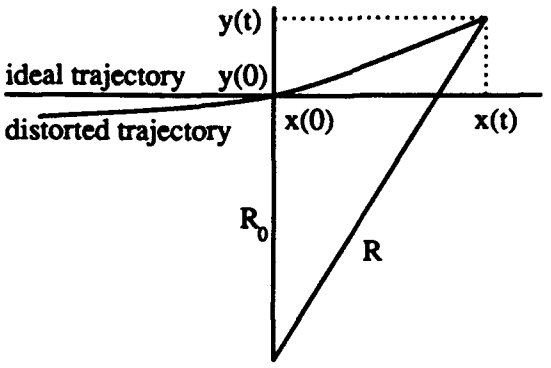

Figure 2.5: Distortion in flight trajectory.

If the parameters Δv, $\frac{\mathrm{d}}{\mathrm{d}t}v$, v_r, $\frac{\mathrm{d}}{\mathrm{d}t}v_r$, $\frac{\mathrm{d}^2}{\mathrm{d}t^2}v_r$ are known, for example by motion measurements, it is possible to compensate the phase error $\varphi_e(t)$. This technique is called motion compensation and is discussed in [18]. Estimation of the phase error from the blurred image is called autofocussing. A great number of estimation techniques is known from the literature [2, 3, 4, 5, 8, 10, 12, 18, 19, 21, 22, 25, 30]. It goes beyond the scope of this document to describe them all, but two main trends in autofocussing will be mentioned. The first one is the mapdrift method [5, 12]. The aperture is sub-divided in several sub-apertures and a multiple look at the same image is performed. Due to the phase errors each map will be shifted relatively from the others. This phase error is determined by cross correlating the maps. The order of the phase error that can be compensated is determined by the number of sub-apertures. A disadvantage of this method is that the azimuth resolution decreases inversely proportional to the number of sub-apertures. The second trend is based on contrast optimization [5, 8, 12, 21]. Methods that use contrast optimization are based on determination of some strongest targets. A disadvantage is that high-clutter or less-contrast images decrease the performance of this method.

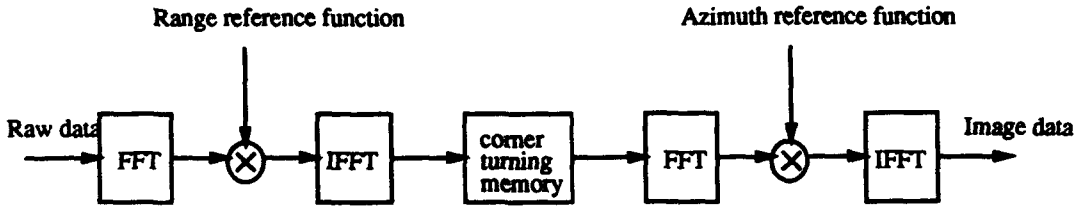

Figure 2.6: SAR processing in FFT domain.

2.2 State of the art

Real-time processing. Real-time[2] SAR processors were first developed in the mid 1970's [16], as a result of the advancement in digital signal processing. The techniques that were used until now remianed more or less unchanged. In most cases pulse compression and azimuth compression are performed in the frequency domain, as is shown in figure 2.6. Proposed architectures are based on FFT processing [6, 9, 11, 13, 23, 24, 27, 31]. Due to the progress in the field of VLSI for FFT processing and array processing the performance of the architectures increased. A few proposed architectures use other transformation techniques, like polynomial and Fermat number transforms [7, 28]. Implementation of the architectures have resulted in parallel processors and computer systems.

The computational complexity of architectures based on FFT processing is still too high for direct VLSI implementation. To illustrate this an example is given. Successively single pulse echoes are sampled and pulse compressed. Let n, $n = \cdots, -1, 0, 1, \cdots$ denote the n^{th} transmitted and received pulse. Let the M samples of echo n (after pulse compression) be stored in a vector $\mathbf{v}_n$. Let the image line l refer to the pixel values of the points $(x_l, y_m, 0)$, $m = 1, \cdots, M$. Azimuth compression to obtain image line l requires $N+1$ pulse echoes $\mathbf{v}_{l-n}$, $n = -N/2, \cdots, N/2$. The next image line $l+1$ requires the N pulse echoes $\mathbf{v}_{l-n}$, $n = -N/2+1, \cdots, N/2$ plus the echo of the next pulse $\mathbf{v}_{N/2+1}$. Hence a continuous storage of $N+1$ vectors is required to perform azimuth compression, which

[2]Real-time processing can be performed on-board or off-board. Since efficient operational real-time on-board SAR processing systems have not been presented yet in the literature, both aspects of real-time processing shall be discussed.

corresponds to storage of $N + 1 \times M$ samples in the corner turning memory, with N and M both of order 10^3. Note that within the interpulse time (of order 10^{-3}) this data has to be shifted, loaded from memory to processor and processed. Since processing is usually done in frequency domain this implies an order of $M(N + 1)\log(N + 1)$ computations per image line necessary to perform the FFT's (note that pulse compression requires an additional $M \log M$ computations).

Real-time systems. Three representative examples of real-time SAR systems (ordered chronologicallly on date of publication) are:

1. (1982) A real-time spaceborne SAR system for off-board SAR procesing is presented in [31]. It is used to process raw SAR data from the SEASAT satellite. The system configuration consists of a minicomputer that acts as a host for three parallel array processors, two disks for data storage and one disk for software storage. The system is software oriented. The processing time for a single-look image[3] (1.2×10^6 pixels) is 90 seconds and the throughput rate is 6700 pixels per second.

2. (1987) A modular reconfigurable real-time spaceborne SAR system is proposed in [9]. It is tested on raw SAR data from the SEASAT satellite. The system consists of three devices: a corner turning memory (DRAM's), an FFT processor (2μ CMOS VLSI technology) and a systolic processor. The processing is broken up in five steps: 1. FFT of echo data, 2. pulse compression, IFFT and storage in corner turning memory, 3. FFT of azimuth data, 4. phase correction, azimuth compression and IFFT, 5. incoherently summing of multiple look-data. Each step requires a recirculation through the SAR processor: from memory through systolic processor and FFT processor and back to memory. The processing of 16×10^6 samples of raw data into one four-look image takes 2 seconds. The proposed SAR processor architecture is an off-board processor.

3. (1989) A real-time on-board SAR system is proposed in [23]. A mesh connected SIMD architecture is used to meet the real-time requirement. The configuration

[3] A look is an image that results from the azimuth processing of the data of a (sub-)aperture. A single-look image is the result of azimuth processing of the complete aperture data. A multiple-look image is the result of the azimuth processing of the data of multiple sub-apertures. The resulting images of the sub-apertures are summed incoherently to obtain the complete image.

consists of a host, a processor array, a data memory, a program memory and a processor array control unit. The processor array contains 64 x 64 mesh connected custom processor elements (1,2μ CMOS VLSI technology). The processing of 16×10^6 samples of raw data into one single-look image takes 1 second. The system follows a maximal pulse repetition frequency of 1000Hz. The implementation has resulted in a prototype on-board SAR processor. The performance meets the real-time requirement theoretically, but power consumption and small-size hardware implementations have not been met yet. An attempt will be made to implement the processor array on a stack of interconnected silicon wafers.

Discussion. From the examples follows that the trends in real-time SAR processing are: increasing the processing speed (from "almost" real-time to real-time) and decreasing the size of the system (from software to hardware oriented systems). The only serious attempt to realize an on-board real-time SAR processor that is found in the literature is outlined in the last example, although it has not yet resulted in an operational system. Processing in FFT domain however might not be the most efficient solution to reduce the computational complexity and the use of memory. It is remarkable that hardly any attempt is made to find alternative approaches for processing in FFT domain. Time domain solutions may be more sophisticated with the present-day techniques for parallel algorithm design. Therefore a new direction in real-time SAR processing can be the development of alternative algorithms for SAR processing. More significant performance improvement would be obtained by the design of algorithms which are optimized in terms of parallelization and pipelinabillity. The basis for this project is therefore to design new algorithms for SAR processing.

2.3 Framework within TNO-FEL

Physics and Electronics Laboratory. The Physics and Electronics Laboratory (FEL) is one of the three institutes of the TNO Division for Defense Research in the Netherlands. Most of its research and development is sponsored by the Ministry of Defense, but TNO-FEL also teams up with industry in national and international defence related and civil projects. TNO-FEL is organized into four research divisions and one division for

technological developments. These are:

1. Operational Research
2. System Development and Information Technology
3. Radar and Communications
4. Physics and Acoustics
5. Technological Developments

PHARUS. TNO-FEL, the National Aerospace Laboratory (NLR) and the Delft University of Technology (faculty of Electrical Engineering, section Microwave Technology and Telecommunication) started several years ago a plan for the development of a C-band airborne SAR, the so-called PHARUS (PHased ARray Universal Sar) [14]. The final goal of *the project is* a full polarimetric C-band ($\lambda = 0.056m$) airborne SAR. The system will be ready in 1994. It will possess an active phased array patch antenna, which enables flexibility in imaging modes in addition to the ability to choose the resolution. Furthermore, the antenna pointing on-board the moving aircraft is maintained through the phased array, rather than by mechanical stabilization. The system that is being developed will be used to investigate military and civil applications, mainly in the field of remote sensing (earth observation). PHARUS is a system that requires off-line SAR processing. Its power is that it can transmit and receive two orthogonal polarizations. Since the brightness of reflectors in a radar image depends on polarization, the contrast can be optimized and reflectors may be classified or even identified.

Before the PHARUS system will be constructed, experience in the field of SAR systems was gained by the development of a limited prototype system, called PHARS, meant as a testbed. The PHARS is not polarimetric. This system was completed recently. The PHARS records a swath width (image strip) of 7 km at a maximum range of 13 km. The azimuth resolution is 1.2 meter (single look). The range resolution is 4.8 meter. The system is flown on a Swearingen Metro, NLR's laboratory aircraft, at altitudes up to 6 km and speeds up to 120 m/s. The incident angle can be varied between 20 and 60 degrees.

To keep in touch with on-line SAR processing TNO-FEL started with the development of an on-line real-time SAR processor. The purpose of this processor is to display on-line an image of the illuminated strip. The SAR processor will be used for general purpose stripmap SAR processing. The PHARS is used as a testbed for the SAR processor. In the future the experience gathered with the SAR processor will be used to develop a complete real-time on-board polarimetric SAR system.

3 PROJECT DESCRIPTION

3.1 Objectives

Main objective: *The definition, design and realization of an on-board real-time synthetic aperture processor within the present-day or near-future state of the technique, especially digital signal processing and VLSI array processing.*

Sub-objectives: The main objective can be refined in the following sub-objectives:

- To decrease the costs of SAR data acquisition such that a real-time on-board SAR processor can be realized.
- To combine expertise on the fields of signal processing, signal processing applications (radar) and VLSI array processing such that the leading positions in these fields will be maintained.
- To obtain a PhD graduation.

3.2 Results

The project has the following intended results:

- **A real-time SAR processor definition is given. The definition should be as broad as possible. Restriction due to hardware limitations are omitted.**
- **A real-time on-board SAR processor is designed and realized. This processor should be an implementation derived from the definition. The processor displays a "quick-look" SAR image. Quick-look means that quality and resolution are of less importance. A global view of the illuminated area is displayed. The equipment can be checked on-line whether it functions well or not. The SAR data can be judged on its usefulness by using the information of the quick-look SAR image.**

- SAR processing as an application of digital signal processing and VLSI array processing is better understood. The project increases insight in:
  1. problems that occur in applications of digital signal processing and VLSI array processing (especially SAR processing).
  2. the design methodology of VLSI array processors for these applications.
- TNO-FEL (applied research and development) and the Delft University of Technology (basic research) combine their expertises on the fields of signal processing, signal processing applications (radar) and VLSI array processing. The leading position of TNO-FEL in the field of SAR processing and related fields, and the leading position of the Delft University of Technology in the field of signal processing and VLSI array processing are maintained.
- The research is presented in leading signal processing and radar magazines and conferences.
- A PhD thesis.

3.3 Conditions and requirements

Functional requirements.

Airborne: The SAR processor will be used for an airborne SAR.

Real-time: After receiving the data it must be processed and displayed instantaneously.

On-board: Processing is done on the aircraft.

Operational requirements.

Image quality: The a SAR processor must display an image that has at least quick-look quality, which means that image quality and resolution are of less importance. A global view of the illuminated area is displayed. It must be possible to check the

equipment on-line whether it functions well or not and to judge the SAR data on its usefulness. The image quality norm may be increased, as long as the data is real-time processed.

Motion compensation (optional): The quality of the image can be improved by phase error compensation with motion data of the antenna and the aircraft. Motion compensation is implemented if real-time processing is possible and if quality improvement is necessary.

Autofocussing (optional): The quality of the image can also be improved by autofocussing. The conditions for implementation are the same as for motion compensation.

Design requirements.

VLSI array processing: The algorithms for SAR processing must provide a high throughput of SAR data. To achieve this, the algorithms are parallelized as much as possible and mapped on array processor architectures. An ideal real-time on-board SAR processor will be small, which implies a realization in VLSI array processors.

Application specific IC's (ASIC's): To meet the previous requirement a choice is made for an application specific VLSI implementation. In this way, speed and complexity can be optimized as much as possible.

3.4 Project outline

The project consists of the definition, design and realization of a real-time SAR processor. The main result of the design of the real-time SAR processor is an operational processor. The first stages of the design trajectory shall be much the same as the first stages of the research trajectory. Basic algorithm and architecture design is required to come to this result. The architecture design stage results in a theoretical real-time SAR processor. In the first stages also a statement about the feasibility of motion compensation and autofocussing is made, based on research. The next stages will lead to an implementation and a realization of the SAR processor. The activities are focussed on the application.

A lay-out is designed and the SAR processor is manufactured. The processor is tested and documented. The last stages differs from the research trajectory since theory is less important in the realization of an operational product. The design trajectory of the real-time SAR processor is subdivided in the following stages:

1. Algorithm design
2. Architecture design
3. Lay-out design
4. Implementation and realization
5. Testing
6. Documentation

The research is focussed mainly on algorithm design and architecture design. The theoretical results will be published. The intention is that this will lead to an PhD graduation. A detailed description of the project stages is found in the next two chapters. In chapter 6 the research and PhD graduation are described in detail.

4 PROJECT STAGES

4.1 Algorithm design

Activities. Algorithms for SAR processing, motion compensation and autofocussing are studied extensively. Experience is obtained in the field of SAR processing. Useful algorithms are selected. The following stages are distinguished:

Literature study: Information about conventional SAR processing, motion compensation and autofocussing is collected. Several digital signal processing algorithms are studied.

Analysis: The echo signal including phase errors is analyzed. A matrix description of the signal is derived. The echo signal is of a convolution of the transmitted signal (including atmospherical loss, antenna pattern, etc.) and the reflectivity function of the illuminated surface. The reflectivity function contains the geometrical information of the surface.

Synthesis: An inverse operation is derived to restore the information of the earths surface. A parallel algorithm is determined that performs this algorithm efficiently.

Tools. The theoretical background to perform the activities mainly consists of synthetic aperture radar theory and linear algebra. Software tools for simulation and verification of algorithms are MatLab, C-programming language and other simulation tools. Hardware tools are a SUN Sparc2 station, personal computers and a Convex supercomputer. The algorithms are tested on SAR data from the PHARS.

Results. The results of this stage will be a set of parallel algorithms to perform real-time SAR processing, which can be mapped on parallel VLSI array architectures.

4.2 Architecture design

Activities. The main activity is the mapping of the algorithms from the first stage onto array architectures. This is done in different stages [17]:

Dependence graph (DG) design: The algorithms of the previous stage are graphical represented. The graph shows the dependence of the computations that occur in the algorithms.

Mapping the DG onto an array architecture: The regularity of the DG is investigated and the best mapping methodology is determined. One or more array processors are designed.

Tools. The behavior of the architecture design is simulated on different levels with high level simulation languages. It is tested on the SAR data from the PHARS.

Results. The architecture design stage results in a array processor architectures. Their behavior and interconnections are described in detail. The architecture is specified in processing units, control units, data busses, etc..

4.3 Lay-out design

Activities. The processing units are investigated on feasibility. A relation between accuracy and SAR resolution on the one side and and processing speed and circuit area on the other side is determined. An optimum is determined which satisfies the requirements. The arithmetic, datacommunication, types of computations, control methodology, etc. are specified from the requirements. Before the actual hardware design is started the implementation of processing units, memory units, control units, etc. are specified. Alternative implementations are for example ASIC's (Application Specific Integrated Circuits), transputers, general purpose DSP's. After this specification the actual hardware components are designed. ASIC design results in a lay-out, transputer and general purpose DSP design result in programming code.

Tools. The components and the system are designed with hardware simulation languages. Lay-out is designed with (graphical) lay-out design systems.

Results. The result is a set of hardware components, specified and designed, and a system design. The complete design is tested on SAR data.

4.4 Implementation and realization

Some hardware components like general purpose DSP's and transputers are bought from external suppliers. The programming is carried out at TNO-FEL. ASIC's are manufactured externally. The whole system is assembled at TNO-FEL. During the previous stages this stage will be specified in detail.

4.5 Testing

Each design stage has its own test and verification run. The designs are tested off-line on SAR data. This raw SAR data has been recorded during testflights with the PHARS. The several components of the system are tested separately. The complete system is tested off-line on SAR data. At the moment the collected SAR data from the PHARS is recorded on-line on a high-speed taperecorder. To test the real-time SAR system on board the SAR data will also be sent on-board to the SAR processor for immediate processing and displaying.

4.6 Documentation

Each stage is documented in a FEL-report. At the end of the documentation stage a coherent document is produced. This document describes the design trajectory, the system and its specifications and the user specifications.

5 PROJECT MANAGEMENT

5.1 Time planning

The time planning of the project is shown in figure 5.1. Because algorithm and architecture design are closely related, a large overlap in time between the the two stages is reserved. Additional to the project stages time is reserved for the writing of the PhD thesis. Parallel to the project stages, time is reserved for literature study and writing of publications. These activities can be considered as part of the subsequent stages.

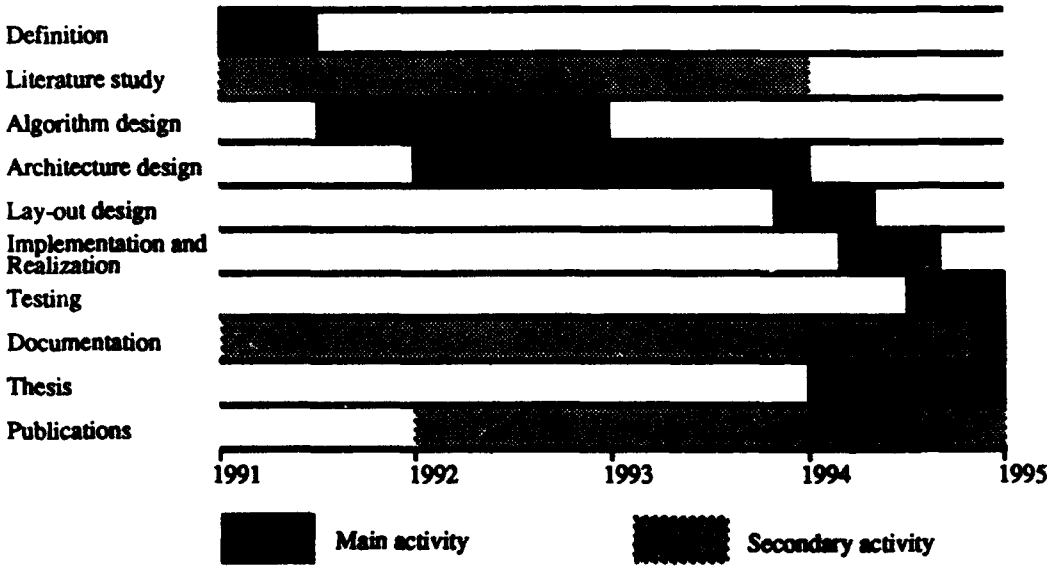

Figure 5.1: Project planning.

5.2 Quality

Two quality norms are defined to meet the requirements. The first deals with the hardware, the second with the image:

Hardware quality: In order to perform real-time on-board SAR processing the hardware must be capable of processing the SAR data efficiently and fast. This results in the following issues during the design stages:

1. The algorithms must be regular and parallel and have low computational complexity
2. The architectures must be parallel, pipelined and dedicated to array processing
3. The lay-out must be dedicated to VLSI array processing

Image quality: The image must have at least quick-look quality, which means that image quality and resolution are of less importance. A global view of the illuminated area is displayed. It must be possible to check the equipment on-line whether it functions well or not and to judge the SAR data on its usefulness. The image quality norm may be increased, as long as the data is real-time processed.

5.3 Communication and information

The scheme in figure 5.2 describes the information flow in terms of input and output per stage (the output information that is used as input for the next stage is marked by dotted arrows). The input and output items shall be described briefly:

Requirements: The requirements are defined in advance (chapter 3).

Theory: The theory describes why a particalar algorithm, architecture or lay-out is chosen.

Methodology: The methodology describes how a particalar algorithm, architecture or lay-out is designed.

Simulated behavior: The simulated behavior is the result of the simulation runs.

Specifications: The specifications are derived from the simulated behavior and the physical constraints, i.e. they are updated after each stage.

Bill of materials: The bill of materials is a list of all necessary components (including software modules).

Assembly instructions: The assmebly instructions give the necessary information to assemble the processor.

Expected behavior: From the specifications of the software and hardware the expected behavior of the processor can be derived.

Test instructions: The test instructions give the necessary information to test the processor.

	Input	Output
Algorithm design	*Requirements (ch. 3)	*Theory *Methodology *Simulated behavior *Specifcations *Algorithm
Architecture design	*Requirements (ch. 3) *Specifcations *Algorithm	*Theory *Methodology *Simulated behavior *Specifcations *Architecture
Lay-out design	*Requirements (ch. 3) *Specifcations *Architecture	*Theory *Methodology *Simulated behavior *Specifcations *Lay-out
Implementation and realization	*Requirements (ch. 3) *Specifcations *Lay-out	*Bill of materials *Assembly instructions *Expected behavior *Specifications
Testing	*Requirements (ch. 3) *Expected behavior *Specifications	*Test instructions *Measured behavior and specifications
Documentation	*All documents previous stages	*Document

Figure 5.2: Information flows.

Measured behavior and specifications: From the testruns the actual behavior and specifications are obtained.

The remaining items are trivial. After each stage the output information is documented. In the documentation stage the information of all stages is collected and documented. Project progress is reported to the project manager (Ir. H. van Es), and research progress to the promotor (Prof.Dr.Ir. P.Dewilde).

5.4 Organization

The project is carried out in service of TNO Physics and Electronics Laboratory (TNO-FEL). The research is carried out in corporation with the section Network Theory of the Delft University of Technology (TUD). The organization of the project is as follows:

Project manager: Ir. H. van Es (TNO-FEL)

Promotor: Prof.Dr.Ir. P. Dewilde I(TUD)

Mentor: Dr.Ir. E. Deprettere (TUD).

Project executor: Ir. L. Bierens (TNO-FEL).

6 RESEARCH

6.1 Research area

As mentioned in chapter 3 the goal of this project is to come to a definition of processor for high performance real-time on-board SAR processing. Due to the great number of data and the high computational complexity conventional algorithms are inadequate to perform this kind of SAR processing. The mapping of these algorithms on new architectures might increase the performance but not sufficiently enough to meet the demands. Therefore the first part of the research of this project is focussed on algorithm design. The second part of the research is focussed on mapping the algorithms on new architectures. The theory for the algorithm design is found in the fields of synthetic aperture radar, linear algebra and digital signal processing. Many algorithms for digital signal processing applications are derived with linear algebra techniques such as matrix computations. However, this approach is rare in SAR processing. The advantage of the use linear algebra is that algorithms are forced to be highly regular. These algorithms can be mapped on high performance array architectures via a systematical design methodologies [17].

6.2 Research description

The research will be carried out mainly in the algorithm design and architecture design stages. In the last year of the project additional time is reserved for the writing of the PhD thesis.

Algorithm design. In the algorithm design stage the following research activities can be distinguished:

1. As preparation for the actual research a literature study to matrix computations, array processing, SAR processing, etc. is carried out.
2. Conventional approaches assume that transformation of the SAR signal to another domain (for example FFT domain) is necessary to perform operations as pulse and

azimuth compression. With linear algebra techniques the transformation may be avoided and processing can be done in time domain. To investigate the possibilities of time domain processing an analysis of the raw SAR signal is required.

3. After the raw SAR data is described, SAR processing algorithms are designed. The requirements for these algorithms are regularity, parallelism and low computational complexity.

Architecture design. In the architecture design stage the algorithms from the previous stage are mapped on array architectures. This requires a detailed analysis of dependencies of computations that occur in the algorithm. The dependence graphs are mapped on signal flow graphs. Finally the signal flow graph are mapped on array processor.

PhD thesis. The intention is that the research leads to a PhD graduation. Therefore additional time is reserved for the writing of a PhD thesis.

Parallel to the activities in each stage, there will be secondary research activities. These activities are:

- a literature study to keep knowledge up-to-date (i.e continuation of the literature study from the first stage).
- the writing and preparation of publications, for example in digital signal processing and remote sensing magazines and on conferences.

6.3 Organization of the PhD graduation

The research is carried out in cooperation with the section Network Theory of the Delft University of Technology (TUD). Prof.Dr.Ir. P. Dewilde will act as promotor and Dr.Ir. E.Deprettere will act as mentor. Formal reporting will be done once in two months globally. Informal discussions will take place more frequently.

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Group Leader
H.R. van Es

Author
L.H.J. Bierens

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A REAL-TIME SYNTHETIC APERTURE RADAR PROCESSOR: INTRODUCTION AND PROJECT DESCRIPTION

11. AUTHOR(S)

L.H.J. BIERENS

12. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

TNO PHYSICS AND ELECTRONICS LABORATORY, P.O. BOX 96864, 2509 JG THE HAGUE
OUDE WAALSDORPERWEG 63, THE HAGUE, THE NETHERLANDS

13. SPONSORING/MONITORING AGENCY NAME(S)

TNO PHYSICS AND ELECTRONICS LABORATORY, THE HAGUE, THE NETHERLANDS

14. SUPPLEMENTARY NOTES

15. ABSTRACT (MAXIMUM 200 WORDS, 1044 POSITIONS)

THIS REPORT PRESENTS A PROJECTS DESCRIPTION FOR THE DESIGN AND REALIZATION OF A REAL-TIME SYNTHETIC APERTURE RADAR (SAR) PROCESSOR. THE PRINCIPLES OF SAR PROCESSING AND THE STATE OF THE ART ARE DESCRIBED. CONVENTIONAL SAR PROCESSING TECHNIQUES DEPEND LARGELY ON FFT TRANSFORMATION TECHNIQUES AND DEVICES. THESE OFFER LIMITED POSSIBILITIES TO INCREASE SPEED AND PERFORMANCE OF A SAR PROCESSOR. THEREFORE THE DESIGN OF NEW ALGORITHMS RATHER THAN ARCHITECTURES OF EXISTING ALGORITHMS IS SUGGESTED. AFTER THAT NEW ARCHITECTURES WILL BE DESIGNED DEDICATED TO THE NEW ALGORITHMS. BY EXPLORING PARALLEL STRUCTURES OF THE ALGORITHMS AND BY USING VLSI ARRAY PROCESSING, SPEED AND PERFORMANCE CAN BE INCREASED SIGNIFICANTLY. THE INTENTION IS THAT THE PROJECT WILL LEAD TO A PHD GRADUATION.

16. DESCRIPTORS	IDENTIFIERS
SYNTHETIC APERTURE RADAR SIGNAL PROCESSING DESIGN ALGORITHMS	DIGITAL SIGNAL PROCESSORS

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